



13th Annual IEEE International ASIC/SOC Conference

September 13-16, 2000

Crystal City Hyatt Hotel, Arlington, VA

Sponsored by the IEEE Circuits and Systems Society
and the IEEE Rochester Section



CONFERENCE-AT-A-GLANCE

Wednesday, September 13

Registration	7:00 a.m. - 5:00 p.m.		
Continental Breakfast	7:00 a.m. - 8:00 a.m.		
Plenary Session	8:10 a.m. - 11:30 p.m.	<i>Keynote: John Kelly, General Manager IBM Microelectronics</i>	
		<i>Plenary Talk: Wolfgang Roethig, NEC</i>	
Open Lunch	11:30 p.m. - 1:30 p.m.		
Exhibits	11:30 p.m. - 6:30 p.m.		
Technical Program	1:30 p.m. - 5:15 p.m.	<i>WP1: Imaging</i>	<i>WP2: Embedded RAM</i>
		<i>WP3: Digital Systems</i>	<i>WP4: Wireless & Portable</i>
Opening Reception	5:15 p.m. - 6:30 p.m.		
Panel Discussion	6:30 p.m. - 8:00 p.m.		

Thursday, September 14

Registration	7:30 a.m. - 5:00 p.m.		
Continental Breakfast	7:30 a.m. - 8:15 a.m.		
Technical Program	8:15 a.m. - 12:00 p.m.	<i>TA1: IP Core Design</i>	<i>TA2: Circuit Design/Mixed Signals</i>
		<i>TA3: IP Des. Methodol.</i>	<i>TA4: Co-Design</i>
		<i>TA5: Modeling & Reuse</i>	
Conference Luncheon	12:00 p.m. - 1:30 p.m.	<i>Luncheon Speaker: James Urquhart, COO, ARM</i>	
Technical Program	1:30 p.m. - 5:15 p.m.	<i>TP1: Modeling & Reuse</i>	<i>TP2: Applications I</i>
		<i>TP3: Building Blocks</i>	<i>TP4: Applications II</i>
Exhibits	9:55 a.m. - 6:00 p.m.		
Buses Depart for Cruise	5:45 p.m.		
Dinner Cruise	6:30p.m. - 10:00 p.m.		

Friday, September 15

Registration	8:00 a.m. - 3:30 p.m.		
Technical Program	8:15 a.m. - 12:25 p.m.	<i>FA1: Low Power</i>	<i>FA2: Physical Design</i>
		<i>FA3: Low Power</i>	<i>FA4: Signal Integrity</i>
		<i>FA5: Formal Methods</i>	
Open Lunch	12:25 p.m. - 1:30 p.m.		
Technical Program	1:30 p.m. - 3:35 p.m.	<i>FP1: High Performance</i>	<i>FP2: Synthesis & Back End</i>

Saturday, September 16

Registration	7:30 a.m. - 1:00 p.m.
Continental Breakfast	7:30 a.m. - 8:00 a.m.
Tutorial Workshops	
Morning Sessions	8:00 a.m. - 12:00 p.m.
Afternoon Sessions	1:00 p.m. - 5:00 p.m.

GENERAL INFORMATION

Location: Hyatt Regency Crystal City at
Reagan National Airport
7799 Jefferson Davis Highway
Arlington, Virginia 22202
703-418-1234

REGISTRATION: For Advance Registration, complete the Registration Form (see centerfold) and mail the form with payment to the Conference Headquarters. Advance registration forms must be received by the Conference Headquarters NO LATER THAN AUGUST 18, 2000. After August 18, you must register at the Conference and pay the late registration fee. Short Course Tutorial participants must register in advance. On-site tutorial registration will only be accepted based on space availability.

IEEE Members: In order to qualify for the membership fees, you must list your IEEE membership number.

CANCELLATIONS: Refund requests must be received, in writing, by August 31 in order to receive a full refund, less a \$50.00 processing fee. Refund requests received after August 31 cannot be guaranteed.

HOTEL RESERVATIONS: A block of rooms has been reserved at the Hyatt Regency Crystal City. To make a reservation, call the hotel at 1-800-233-1234 or 1-703-418-1234 or fax to 1-703-413-6727, make sure to identify yourself as an ASIC/SOC Conference attendee.

Room rates are \$149/single and \$159/double. Reservations must be received by August 18 in order to qualify for these special conference rates.

RESERVATIONS MUST BE RECEIVED BY FRIDAY, AUGUST 18 to guarantee the conference rate.

You will receive a reservation confirmation directly from the hotel. All changes and cancellations should be made directly with the hotel. It is the responsibility of each participant to make changes or cancellations no later than 48 hours prior to scheduled arrival. Room reservations will be held until 6:00 p.m. unless a later time is guaranteed by a credit card. Rooms are generally not available for check-in until 3:00 p.m. on the day of arrival.

SPEAKER READY ROOM: A practice room will be available at the hotel and will be open from 7:30 a.m. - 5:00 p.m. on Wednesday, Thursday and Friday. Use of the room is on an unreserved basis.

SUPPLIER EXHIBITS: Suppliers of products, materials and tools related to ASIC and System-on-Chip design, manufacturing and integration will exhibit their latest offerings on September 13 and 14. If you are interested in participating, contact the Conference Headquarters at 1-301-527-0900 x 104 or email to wendyw@widerkehr.com.

TRANSPORTATION

The Hotel provides complimentary shuttle service between the airport and the hotel. To arrange for a pick-up, at the airport, use the Courtesy Shuttle Telephone located in the baggage area to contact the hotel.

CONFERENCE HEADQUARTERS

Wendy Walker, Conference Manager
ASIC/SOC Conference
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WEDNESDAY, SEPTEMBER 13 - MORNING

Plenary Session
Regency Ballroom AB

- 7:00 a.m. Registration
8:10 a.m. **Opening Remarks**, Thomas Buechner, General Conference Chair
8:20 a.m. **Technical Program Overview**, Jo Dale Carothers, Technical Program Chair
8:30 a.m. **Keynote Address**: "Communications Systems on a Chip: Opportunity and Challenges"
John E. Kelly, III, General Manager, IBM Microelectronics Division
- 9:30 a.m. Break
- 10:00 a.m. **Plenary Talk**: Design for signal integrity on SOC, Wolfgang Roethig, NEC
11:00 a.m. **Exhibitor Presentations**
11:30 p.m. **Open Lunch**
Exhibits Open

WEDNESDAY, SEPTEMBER 13 - AFTERNOON

WP1: IMAGING

Regency Ballroom A

Session Chair: Paul Lee, Eastman Kodak

Session Co-Chair: David England, Intel

- 1:30 p.m. **Design and Synthesis of Built-in Self-Testable Two-Dimensional Discrete Cosine Transform Circuits**, H.B. Kim and D.S. Ha*, Sun Microsystems, Inc., Palo Alto, CA and *Virginia Tech, Blacksburg, VA
WP1.1
- 1:55 p.m. **Switched-Current Filter Design for Image Processing Systems**, A. Handkiewicz, M. Kropidowski, M. Lukowiak, and M. Bartkowiak, Poznan University of Technology, Poznan, Poland
WP1.2
- 2:20 p.m. **A Reconfigurable Pipelined IDCT for Low-Energy Video Processing**, S. Kim, C.H. Ziesler and M.C. Papaefthymiou, University of Michigan, Ann Arbor; MI
WP1.3
- 2:45 p.m. **Fast Digital Photon Correlation System with High Dynamic Range**, M. Engels, B. Hoppe*, H. Meuth, and R. Peters*, University of Applied Science, Darmstadt, Germany and *ALV - GmbH, Langen, Germany
WP1.4
- 3:10 p.m. **Break**

WP2: SPECIAL SESSION: EMBEDDED DRAM

Regency Ballroom B

Session Chair: Shih-Lien Lu, Oregon State University

Session Co-Chair:

- 1:30 p.m. **Overview and Session Summary**, Shih-Lien Lu, Oregon State University
WP2.1
- 1:55 p.m. **Obeying Moore's Law Beyond 0.18 micron**, S. Borkar, Intel Corp., Hillsboro, OR
WP2.2
- 2:20 p.m. **The Ideal SoC Memory: 1T-SRAM**, W. Leung, F.-C. Hsu and M.-E. Jones, MoSys Inc., Sunnyvale, CA
WP2.3
- 2:45 p.m. **An 0.18um Embedded FCRAM ASIC with DRAM Density and SRAM Performance**, Y. Okajima, A. Cosoroaba* and H. Kobayashi*, Fujitsu Ltd., Kawasaki, Japan and *Fujitsu Microelectronics, Sar Jose, CA
WP2.4
- 3:10 p.m. Break

WEDNESDAY, SEPTEMBER 13 - AFTERNOON

WP3: DIGITAL SYSTEMS

Regency Ballroom A

Session Chair: David England, Intel

Session Co-Chair: Sumer Can, Maxim

3:35 p.m. **High-Speed Adder Design Using Time Borrowing and Early Carry Propagation**, G. Jung and
WP3.1 G. Sobelman, University of Minnesota, Minneapolis, MN

4:00 p.m. **Interpolation-Based Digital Quadrature Frequency Synthesizer**, R. Larson and S.-L. Lu,
WP3.2 Oregon State University, Corvallis, OR

4:25 p.m. **On-Chip Delta- σ Noise in the Power Distribution Networks of High Speed CMOS Integrated
Circuits**, K.T. Tang and E.G. Friedman, University of Rochester, Rochester, NY
WP3.3

4:50 p.m. **A System-Level Simulation Environment for System-On-Chip Design**, T. Schneider, J. Madès,
WP3.4 A. Windisch*, M. Glesner, D. Monjau*, and W. Ecker**, Darmstadt University of Technology,
Darmstadt, Germany, *Technical University of Chemnitz, Chemnitz, Germany and **Infineon
Technologies, Munich, Germany

WP4: WIRELESS AND PORTABLE COMMUNICATIONS

Regency Ballroom B

Session Chair: Mark Schrader, Eastman Kodak

Session Co-Chair:

3:35 p.m. **A QAM Modulator for WCDMA Base Station**, J. Vankka, L. Sumanen and K. Halonen, Helsinki
WP4.1 University of Technology, Espoo, Finland

4:00 p.m. **A DFE Equalizer ASIC chip using the MMA Algorithm**, D. Shin, K.H. Park and M.H. Sunwoo,
WP4.2 Ajou University, Suwon, Korea

4:25 p.m. **Vector Quantization Processor for Mobile Video Communication**,
WP4.3 T. Iwahashi, T. Shibayama,
M. Hashimoto, K. Kobayashi, and H. Onodera, Kyoto University, Kyoto, Japan

4:50 p.m. **VLSI Implementation of Portable MPEG-4 Audio Decoder**, S. Hashimoto, A. Niwa, H. Okuhata,
WP4.4 T. Onoye, and I. Shirakawa, Osaka University, Osaka, Japan

5:15 p.m. **Opening Reception**

6:30 p.m. **Panel Discussion: "Moore's Law and Reality - Perspectives in SoC Design"**

to
Chair: Shih-Lien Lu, Oregon State University

8:00 p.m.

Panelists:

Shekhar Borkar, Intel Corp.

Wing Leung, MoSys

Carl Ashley, IBM Microelectronics

Wolfgang Roethig, NEC

THURSDAY, SEPTEMBER 14 - MORNING

TA1: IP CORE DESIGN

Regency Ballroom A

Session Chair: John Chickanosky, IBM

Session Co-Chair: Thomas Büchner, IBM

- 8:15 a.m. **Invited paper: Cultivating the Disciplines of Reusable IP Development : ASIC Cores**
TA1.1 Methodology Initiatives, C. Ashley, E. Keller, O. Strohacker, D. Reed, IBM Microelectronics, Essex Junction, VT
- 8:40 a.m. **Parametrizable Hybrid Stack-Register Processor as Soft Intellectual Property Module**, T. Roewer, P. Luethi, M. Stadler, D. Forrer, and S. Moscibroda, Integrated Systems Laboratory, Zurich, Switzerland
- 9:05 a.m. **HiPAR-DSP - A Scalable Family of High Performance DSP-Cores**, J.P. Wittenburg, W. Hinrichs, H. Lieske, H. Kloos, L. Friebe, and P. Pirsch, University of Hannover, Hannover, Germany
- 9:30 a.m. **Improved VLSI Designs for Multiplication and Inversion in $GF(2^m)$ over Normal Bases**, L. Gao and G.E. Sobelman, University of Minnesota, Minneapolis, MN

TA2: CIRCUIT DESIGN AND MIXED SIGNALS

Regency Ballroom B

Session Chair: P R Mukund, Rochester Institute of Technology

Session Co-Chair: Paul Lee, Eastman Kodak

- 8:15 a.m. **Direct-Conversion Quadrature-Modulator for 0.8-1 GHz with Flip-Chip Passives**, E. Tiiliharju, A. Friman and K. Halonen, Helsinki University of Technology, Helsinki, Finland
- 8:40 a.m. **Optimization of A 0.13um CMOS Backend Interconnect Process for ASIC SOC: Low k Dielectric vs Cu Conductor**, P. Bendix, W. Loh, J.J. Lee, and W. Li, LSI Logic, Milpitas, CA
- 9:05 a.m. **An Efficient Method for Estimating Switching Activity in Arithmetic Circuits Using a Lumped Delay Model**, R. Sridhar, SUNY Buffalo, Buffalo, NY
- 9:30 a.m. **Blind Estimation and Error Correction in a CMOS ADC**, J. Elbornsson, Linköping University, Linköping, Sweden
- 9:55 a.m. **Break**

THURSDAY, SEPTEMBER 14 - MORNING

TA3: IP DESIGN METHODOLOGY

Regency Ballroom A

Session Chair: Dave Braverman, NEC

Session Co-Chair: John Chikanosky, IBM

- 10:20 a.m. **TA3.1** **IVE : An Internet Based distributed VHDL Environment**, K. Yang, A. Windisch*, T. Schneider, J. Mades, M. Glesner, and W. Ecke**, Darmstadt University of Technology, Darmstadt, Germany, *Technical University of Chemnitz, Chemnitz, Germany, and **Infineon Technologies, Munich, Germany
- 10:45 a.m. **TA3.2** **Low Level Watermarking of VLSI Designs for Intellectual Property Protection**, D.L. Irby, R.D. Newbould, J.D. Carothers, J.J. Rodriguez, and W.T. Holman, University of Arizona, Tucson, AZ

TA5: MODELING AND REUSE

Regency Ballroom A

Session Chair: Howard Chen, IBM/T.J. Watson Research Center

Session Co-Chair: Hyun Lee, Lucent Technologies/Bell Labs

- 11:10 a.m. **TA5.1** **Designing Reusable Components in VHDL**, M. Chang and K. Agun, Illinois Institute of Technology, Chicago, IL
- 11:35 a.m. **TA5.2** **A Layered Approach to Behavioral Modeling of Bus Protocols**, S. Chonnad and B. Needamangalam, Synopsis, Inc., Mountain View, CA

TA4: CODESIGN: CASE STUDIES AND METHODOLOGIES

Regency Ballroom B

Session Chair: Cherrice Traver, Union College

Session Co-Chair: Wolfram Hardt, University of Paderborn

- 10:20 a.m. **TA4.1** **Robust Mobile Computing - A Case Study in Architecture Performance Evaluation**, R. Kress and S. Schulz*, Infineon Technologies, Munich, Germany and *University of Arizona, Tucson, AZ
- 10:45 a.m. **TA4.2** **SOC-Driven Design Methodology for Full Custom High Performance Mixed-Signal Designs**, R. Wittmann, W. Schardein*, D. Bierbaum, and M. Darianian, Nokia Research Center, Bochum, Germany and *University of Applied Sciences, Dortmund, Germany
- 11:10 a.m. **TA4.3** **Coware Pipelining for Exploiting Intellectual Properties and Software Codes in Processor-based Design**, H. Choi and I.-C. Park*, Samsung Electronics, Seoul, Korea and *KAIST, Seoul, Korea
- 11:35 a.m. **TA4.4** **Architecture Level Optimization for Asynchronous IPs**, W. Hardt, M. Visarius and B. Kleinjohann*, University of Paderborn, Paderborn, Germany and *C-LAB: Cooperative Computing & Communications Laboratory, Paderborn, Germany

12:00 p.m. **Luncheon with Guest Speaker: James Urquhart, Chief Operating Officer, ARM Holdings**

THURSDAY, SEPTEMBER 14 - AFTERNOON

TP1: MODELING AND REUSE

Regency Ballroom A

Session Chair: Hyun Lee, Lucent Technologies/Bell Labs

Session Co-Chair:

- 1:30 p.m. **Analysis of VHDL Semantics through a High-Level Synthesis Tool**, G. Savaton, E. Casseau and E. Martin, UBS University, Lorient, France
TP1.1
- 1:55 p.m. **Design, Optimization, and Implementation of a Universal FFT Processor**, P. Kumhom, J.R. Johnson and P. Nagvajara, Drexel University, Philadelphia, PA
TP1.2
- 2:20 p.m. **Methodology and Code Reuse in the Verification of Telecommunication SOCs**, O. Petlin, A. Genusov and L. Wakeman*, ASIC-Alliance Corporation, Woburn, MA and *Lucent Technologies, Holmdel, NJ
TP1.3
- 2:45 p.m. **Development and Application of a Macro Model for Flash EEPROM Design**, M. O'Shea, A. Concannon, K. McCarthy, B. Lane, A. Mathewson, and M. Slotboom*, National Microelectronics Research Centre, Cork, Ireland and *Philips Research Laboratories, Eindhoven, The Netherlands
TP1.4

TP2: APPLICATIONS I

Regency Ballroom B

Session Chair: Thomas Büchner, IBM

Session Co-Chair: Dave Braverman, NEC

- 1:30 p.m. **Design of Front-end Processor Core for Max. 64X-Speed CD-ROM Drive System**, A. Wada, T. Otsuka, K. Tani, and T. Sawai, Sanyo Electric Co., Ltd., Gifu, Japan
TP2.1
- 1:55 p.m. **An Embedded PowerPC™ SOC for Test and Measurement Applications**, B. Blaner, D. Czenkusch*, R. Devins, and S. Stever*, IBM Microelectronics, Essex Junction, VT and *Agilent Technologies, Loveland, CO
TP2.2
- 2:20 p.m. **A Mixed-Mode Single-Chip Motor-Drive-Specific Microcontroller with a 12-bit 125KS/s ADC**, J.-C. Kim, S.-H. Lee, J.-Y. Kim, Y.-C. Jang, I.-S. Mok* and H.-J. Park, Postech, Pohang, Korea and *Research Institute of Industrial Science and Technology, Pohang, Korea
TP2.3
- 2:45 p.m. **A 64/256 QAM Receiver Chip for High-speed Communications**, D. Shin, K.H. Park and M.H. Sunwoo, Ajou University, Suwon, Korea
TP2.4
- 3:10 p.m.** Coffee Break

THURSDAY, SEPTEMBER 14 - AFTERNOON

TP3: BUILDING BLOCKS

Regency Ballroom A

Session Chair: Mike Gaboury, Rosemount Inc.

Session Co-Chair: David England, Intel

- 3:35 p.m. **TP3.1** **An Energy-Efficient Leakage-Tolerant Dynamic Circuit Technique**, L. Wang, R.K. Krishnamurthy*, K. Soumyanath, and N.R. Shanbhag, University of Illinois, Urbana, IL and *Intel Corp., Hillsboro, OR
- 4:00 p.m. **TP3.2** **A Program Compression Technique Supporting IP-centric SOC Design**, C. Yeh and C.-S. Wang, National Chung Cheng University, Chia-Yi, Taiwan, ROC
- 4:25 p.m. **TP3.3** **Low-Power 4-Way Associative Cache for Embedded SOC Design**, H. Choi, M.-K. Yim, J.-Y. Lee, B.-W. Yun, and Y.-T. Lee, Samsung Electronics, Seoul, Korea
- 4:50 p.m. **TP3.4** **Digit-Serial Fixed Coefficient Complex Number Multiplier-Accumulator on FPGAs**, T. Sansaloni, J. Valls, and K. Parhi*, University Politecnica de Valencia, Valencia, Spain and *University of Minnesota, Minneapolis, MN

TP4: APPLICATIONS II

Regency Ballroom B

Session Chair: Thomas Büchner, IBM

Session Co-Chair: Dave Braverman, NEC

- 3:35 p.m. **TP4.1** **Low Power Video Object Motion Tracking Architecture**, W. Badawy and M. Bayoumi, RA, Lafayette, LA
- 4:00 p.m. **TP4.2** **Design Self-Synchronized Clock Distribution Networks in an SoC ASIC using DLL with Remote Clock Feedback**, H.Q. Nguyen, H. Lee and D.W. Potter, Lucent Technologies, Allentown, PA
- 4:25 p.m. **TP4.3** **Using Computational RAM for Volume Rendering**, A. Snip, D. Elliott, M. Margala, and N. Durdle, University of Alberta, Edmonton, Alberta, Canada
- 4:50 p.m. **TP4.4** **ICORE: A Low-Power Application Specific Instruction Set Processor for DVB-T Acquisition and Tracking**, T. Gloekler, S. Bitterlich and H. Meyr, Aachen University of Technology, Aachen, Germany
- 5:50 p.m. **Transportation to Dinner Cruise**
- 7:00 p.m. **Banquet - Dinner Cruise**

FRIDAY, SEPTEMBER 15 - MORNING

FA1: LOW POWER: MODELS, ARCHITECTURE AND TOOLS

Washington Room A

Session Chair: Katsu Nakamura, Analog Devices

Session Co-Chair: Mike Gaboury, Rosemount Inc.

8:15 a.m. **Modeling Energy of the Clock Generation and Distribution Circuitry**, D. Duarte, M.J. Irwin and
FA1.1 V. Narayanan, Pennsylvania State University, University Park, PA

8:40 a.m. **Orthogonal Partitioning and Gated Clock Architecture for Low Power Realization of FSMs**, R.
FA1.2 Shelar, H. Narayanan* and M.P. Desai, Silicon Automation Systems, Bombay, India and *Indian
Institute of Technology, Bombay, India

9:05 a.m. **A Complete Model for Glitch Analysis in Logic Circuits**, K.-S. Chung, T. Kim* and C. L. Liu**,
FA1.3 Synopsis, Inc., Mountain View, CA, * KAIST, Taejon, Korea and **National Tsing Hua University,
Hsinchu, Taiwan, ROC

9:30 a.m. **POPS: A Tool for Delay/Power Performance Optimization**, N. Azemard, M. Aline and D.
FA1.4 Auvergne, LIRMM-University of Montpellier, Montpellier, France

FA2: PHYSICAL DESIGN TECHNIQUES

Washington Room B

Session Chair: Richard Auletta, LSI Logic Corp

Session Co-Chair:

8:15 a.m. **Design of a Databus Charge Recovery Mechanism**, V. Narayanan, V. Lyuboslavsky, B. Bishop,
FA2.1 and M.J. Irwin, Pennsylvania State University, University Park, PA

8:40 a.m. **On-Chip Decoupling Capacitor Optimization using Architectural level Current Signature**
FA2.2 **Prediction**, M. Pant, P. Pant and D.S. Wills, Georgia Institute of Technology, Atlanta, GA

9:05 a.m. **Design of Low-Capacitance Bond Pad for High-Frequency I/O Applications in CMOS**
FA2.3 **Integrated Circuits**, M.-D. Ker, H.-C. Jiang* and C.-Y. Chang, National Chiao-Tung University,
Hsinchu, Taiwan, ROC and *ITRI, Hsinchu, Taiwan, ROC

9:30 a.m. **High Level Estimation of the Area and Power Consumption of On-Chip Interconnects**, D.
FA2.4 Langen, A. Brinkmann and U. Rückert, Heinz Nixdorf Institute, Paderborn, Germany

9:55 a.m. **Break**

FRIDAY, SEPTEMBER 15 - MORNING

FA3: LOW POWER CIRCUITS

Washington Room A

Session Chair: Katsu Nakamura, Analog Devices, Inc.

Session Co-Chair: Mike Gaboury, Rosemount, Inc.

- 10:20 a.m. **FA3.1** **Power Optimization of Delay Constrained Circuits**, A. Nayak, M. Haldar, P. Banerjee, C. Chen, and M. Sarrafzadeh, Northwestern University, Evanston, IL
- 10:45 a.m. **FA3.2** **Low-Power Skewed Static Logic (S²L) with Topology-dependent Dual Vt**, C. Kim, J. Lee, K.-H. Baek, and Sung-Mo Kang, University of Illinois, Urbana, IL
- 11:10 a.m. **FA3.3** **Power Optimization of Standard Cell Flip Flops**, B. Rasmussen and J.A. Wright, American Microsystems, Inc., Pocatello, ID

FA5: FORMAL METHODS

Washington Room A

Session Chair: Richard Auletta, LSI Logic Corp

Session Co-Chair:

- 11:35 a.m. **FA5.1** **Model Reductions in MDG-based Model Checking**, J. Hou and E. Cerny, Université de Montréal, Montréal, Québec, Canada
- 12:00 p.m. **FA5.2** **Formal Representation of Gated Clock Designs**, T. Seceleanu and J. Plosila*, Turku Center for Computer Science, Turku, Finland and University of Turku, Turku, Finland

FA4: SIGNAL INTEGRITY

Washington Room B

Session Chair: Ram Sridhar, SUNY at Buffalo

Session Co-Chair:

- 10:20 a.m. **FA4.1** **Characterization of Interconnect Coupling Noise using In-Situ Delay-Change Curve Measurements**, T. Sato, Y. Cao*, D. Sylvester**, and C. Hu, Hitachi, Ltd., Tokyo, Japan, *University of California, Berkeley, CA and **Synopsys, inc., Mountain View, CA
- 10:45 a.m. **FA4.2** **A Differential High-Speed Digital CMOS Buffer with Hysteresis for Improved Noise Immunity**, R. Secaraenu and E.G. Friedman, University of Rochester, Rochester, NY
- 11:10 a.m. **FA4.3** **Capturing Input Switching Dependency In Crosstalk Noise Modeling**, L. Chen, M. Marek-Sadowska, R. Divecha, and P. Singh, University of California, Santa Barbara, CA
- 11:35 a.m. **FA4.4** **Efficient Static Timing Analysis in Presence of Crosstalk**, T. Xiao, C.-W. Chang and M. Marek-Sadowska, University of California, Santa Barbara, CA
- 12:00 p.m. **FA4.5** **An Effective Modeling Technique for the Delay Calculation and the Skew Analysis for Clock Grid Designs**, G. Kim, D.-S. Cho and J.-T. Kong, Samsung Electronics Co., Ltd. Yongin-City, Korea
- 12:15 p.m. **Open Lunch**

FRIDAY, SEPTEMBER 15 - AFTERNOON

FP1: HIGH PERFORMANCE AND LOW POWER

Washington Room A

Session Chair: Ram Sridhar, SUNY at Buffalo

Session Co-Chair:

1:30 p.m. **Dynamic-Threshold CMOS SRAM Cells for Fast, Portable Applications**, A. Bhavnagarwala, A. Kapoor and J.D. Meindl, Georgia Institute of Technology, Atlanta, GA
FP1.1

1:55 p.m. **An Zero-Overhead Self-timed Divider using New Pipeline Scheme**, J.-L. Yang, C.-S. Choy and C.-F. Chan, The Chinese University of Hong Kong; new Territory, Hong Kong
FP1.2

2:20 p.m. **Scalable Binary Sorting Architecture Based on Rank Ordering With Linear Area-Time Complexity**, I. Hatirnaz and Y. Leblebici, Worcester Polytechnic Institute, Worcester, MA
FP1.3

2:45 p.m. **High Throughput FIR Filter Design for Low Power SoC Applications**, A.T. Erdogan and T. Arslan, University of Edinburgh, Edinburgh, United Kingdom
FP1.4

3:10 p.m. **Low Power Controller Optimization Based on Data Path Pattern Extraction**, P.-Q. Zou and C.-Y. Tsui, Hong Kong University of Science and Technology, Hong Kong
FP1.5

FP2: SYNTHESIS AND BACK END TOOLS

Washington Room B

Session Chair: Hyun Lee, Lucent Technology/Bell Labs

Session Co-Chair: Howard Chen, IBM/T.J. Watson Research Center

1:30 p.m. **Right Topologizer: An Efficient Schematic Generator for Multi-level Optimization**, N.-H. Kim, K.-S. Kim, K.-M. Choi, and J.-T. Kong, Samsung Electronics, Yongin City, Korea
FP2.1

1:55 p.m. **Predictable Routing**, R. Kastner, E. Bozorgzadeh and M. Sarrafzadeh, Northwestern University, Evanston, IL
FP2.2

2:20 p.m. **Real Time Application Architectural Synthesis Dedicated to Sub-Micron Technologies**, E. Casseau and J. Martin, UBS University, Lorient, France
FP2.3

2:45 p.m. **Cell Library Development using Multi-Objective Function Optimization**, M. Delaurenti, M. Graziano, G. Masera, G. Piccinini, and M. Zamboni, Politecnico di Torino, Torino, Italy
FP2.4

SATURDAY, SEPTEMBER 16

MORNING TUTORIAL WORKSHOPS

8:00 a.m. - 12:00 p.m.

SOI Design Considerations And System-Level Design

N. Rohrer and K. Bernstein, IBM

Interconnect Modeling and Design for Giga-Hertz Circuits and Systems

Prof. L. He, University of Wisconsin and S. Lin, Hewlett-Packard Laboratories

Design Solutions and Techniques for Vision System On a Chip and Fine-grain Parallelism Integration

F. Paillet, CTA, France and D. Mercier, ENSTA, France

AFTERNOON TUTORIAL WORKSHOPS

1:00 p.m. - 5:00 p.m.

High-performance Low-power Buses

Prof. M. Stan, University of Virginia and Prof. C. K. K. Yang, University of California (UCLA)

Design For Test In Mixed-Signal Circuits

M. Mallinson, Analog Systems

Design Methodologies and CAD Solutions for Managing Noise in SoC Designs

S. McCormick, Sapphire Design Automation,
A. Kahng, University of California (UCLA) and
S. Muddu, SGI